CLAIMS:

1. A processing apparatus, comprising:
- an input means for inputting data;
- a register file for storing said input data;
- at least a first and a second issue slot, wherein each issue slot comprises a plurality of functional units;
and wherein the processing apparatus is conceived for processing data retrieved from the register file based on control signals generated from a set of instructions being executed in parallel, the set of instructions comprising at least a first and a second instruction, the first issue slot being controlled by a first control word corresponding to the first instruction and the second issue slot being controlled by a second control word corresponding to the second instruction,
characterized in that the width of the first control word is different from the width of the second control word.

2. An apparatus according to Claim 1, wherein said processing apparatus is a VLIW processor and wherein said set of instructions is grouped in a VLIW instruction.

3. An apparatus according to Claim 2, wherein the VLIW instruction is a compressed VLIW instruction, comprising dedicated bits for encoding of NOP operations.

4. An apparatus according to Claim 3, comprising a decompression means for decompressing the compressed VLIW instruction and wherein the decompression means is conceived to derive information on the control word width using the dedicated bits.

5. An apparatus according to Claim 1, which further comprises a connection network for coupling the register file and the issue slots.

6. An apparatus according to Claim 2, wherein the register file is a distributed register file.

7. An apparatus according to Claim 1, wherein the width of the first and the second control word is an integer multiple of a predetermined value.

8. A processing method for processing data, said method comprising the following steps:

- storing input data in a register file;
- processing data retrieved from the register file based on control signals generated from a set of instructions being executed in parallel, the set of instructions comprising at least a first and a second instruction, a first issue slot being controlled by a first control word corresponding to the first instruction and a second issue slot being controlled by a second control word corresponding to the second instruction,

and wherein the first and the second issue slot comprise a plurality of functional units, characterized in that the width of the first control word is different from the width of the second control word.

9. A method according to Claim 8, wherein said set of instructions is grouped in a VLIW instruction.

10. A method according to Claim 9, wherein the VLIW instruction is a compressed VLIW instruction, comprising dedicated bits for encoding of NOP operations.

11. A method according to Claim 10, further comprising the step of decompressing the compressed VLIW instruction by means of a decompression means, and wherein the decompression means derives information on the control word width using the dedicated bits.

12. A compiler program product for generating a sequence of sets of instructions, a set of instructions being arranged for parallel execution, the set of instructions comprising at least a first and a second instruction, characterized in that the generated sequence of sets of instructions is arranged for execution by a processing apparatus comprising at least a first and a second issue slot, the first issue slot controlled by a first control word corresponding to the first instruction and the second issue slot controlled by a second control word corresponding

to the second instruction, the width of the first control word being different from the width of the second control word.

13. A computer program comprising computer program code means for instructing a computer system to perform the steps of the method according to Claim 8.

14. An information carrier comprising a sequence of sets of instructions, a set of instructions being arranged for parallel execution, the set of instructions comprising at least a first and a second instruction, characterized in the generated sequence of sets of instructions is arranged for execution by a processing apparatus comprising at least a first and a second issue slot, the first issue slot controlled by a first control word corresponding to the first instruction and the second issue slot controlled by a second control word corresponding to the second instruction, the width of the first control word being different from the width of the second control word.